

REMARKS

Claims 1-20 remain pending in the current Application. No amendments to the claims have been made herein. The specification has been amended at page 12, line 29, to correct a typographical error by replacing "abodiments" with "embodiments", as requested by the Examiner. The specification has also been amended at page 12, line 31, to correct another typographical error by replacing "prediciton" with "prediction".

Applicants submit that the amendments do not add new matter to the current Application. All the amendments herein have been made in order to clarify the claims and not for prior art reasons. Applicants also submit that (1) no amendment made was related to the statutory requirements of patentability unless expressly stated herein, and (2) no amendment made was for the purpose of narrowing the scope of any claim, unless Applicants have argued herein that such amendment was made to distinguish over a particular reference or combination of references.

Rejection of claims 2-5 and 13 under 35 U.S.C. 112

Applicants submit that claims 2-5 and 13, as filed, are patentable under 35 U.S.C. 112. The Examiner states that it is not clear whether the "control circuitry" is an element of the "instruction fetch unit" because the "control circuitry" is claimed as an independent element. As the Examiner points out in FIG. 2 of the current Application, the "control circuitry" (216) is one of the elements inside the "instruction fetch unit" (220); however, FIG. 2 illustrates just one embodiment where the control circuitry may be located in instruction fetch unit 220. That is, in alternate embodiments, the control circuitry may be located outside the instruction fetch unit, as clearly covered by claims 2-5 and 13 as filed, so long as it still provides the desired functionality. Furthermore, the "control circuitry" (216) is still an element within the central processing unit (as claimed in claims 2-5 and 13), regardless of whether it is located within the instruction fetch unit or not. Therefore, Applicants submit that claims 2-5 and 13 are patentable under 35 U.S.C. 112.

Rejection of claims 1, 2, 7-13, and 15-20 under 35 U.S.C. 102

Applicants respectfully submit that claims 1, 2, 7-13, and 15-20 are patentable over Great Britain Patent No. 2, 283, 595 (hereinafter referred to as GB '595)

Claims 1, 2, and 7-9

Applicants submit that claim 1 is not taught or suggested by GB '595. Claim 1, as filed, claims a data processing system having a first and a second mode of operation where the first mode of operation utilizes branch prediction and the second mode of operation utilizes substantially no branch prediction. This is not taught or suggested by GB '595. GB '595 teaches two branch prediction modes: a static branch prediction mode and a dynamic branch prediction mode, where branch prediction is performed in *both* modes. That is, data processor 10 of GB '595 always performs branch prediction (either static or dynamic) regardless of the operating mode. (See e.g. page 5, lines 5-22, of GB '595.) The Examiner cites page 15, lines 30-35, and page 16, line 1, which discusses the taken/not-taken bit which determines whether the branch prediction logic unit 72 will select the next address generated by sequential address calculator 72 or branch address calculator 74. However, this is describing operation of the static branch prediction mode which still performs branch prediction (see lines 17-35 of page 15 of GB '595). Note that branch prediction includes predicting whether or not a branch instruction will be taken before the condition on which the instruction is based is known (see Abstract of GB '595). That is, branch prediction includes predicting whether or not to take a branch (see, e.g., line 25-27 of page 15 of GB '595). Therefore, the single taken/not-taken bit is used within the static branch prediction mode to determine how to generate the next address (based on whether the branch is predicted to be taken or not, which is based on the branch prediction algorithm used.) Therefore, GB'595 does not teach or suggest a mode of operation which utilizes substantially no branch prediction (for example, see page 8, line 26, through page 9, line 6, and FIG. 3 of the current Application for an example of operation when substantially no branch prediction is being used). Therefore, for at least these reasons Applicants submit that GB '595 does not teach or suggest claim 1.

Claims 2, and 7-9 have not been independently addressed because they depend directly or indirectly from allowable claim 1, and are therefore allowable for at least those reasons stated above with respect to claim 1.

Claims 10-13 and 15-20

Applicants submit that claims 10 and 16 are not taught or suggested by GB '595. Claims 10 and 16, as filed, relate to a data processing system having a first and a second mode of operation where the first mode of operation results in a first address setup timing and the second mode of operation results in a second address setup timing that allows for an earlier address valid time as compared to the first address setup timing. This is not taught or suggested by GB '595. The Examiner cites the single taken/not taken bit as the first signal which enables the first or second mode of operation. However, the states of the single taken/not-taken bit are used to predict whether the branch is taken or not and does not affect timing of the address valid time. That is, the single taken/not-taken bit is used to determine how to generate the next predicted address (whether it is a sequential address or a branch target address) where the timing of the next predicted address is not affected by this single taken/not-taken bit. The Examiner proceeds to cite "the first mode of operation utilizes branch prediction at the earlier time, see page 5, line 15". However, the "earlier time" cited on page 5, line 15, of GB '595 does not refer to two operating modes where one results in an earlier address valid time, but instead refers to the earlier time at which an address is predicted (regardless of the branch prediction mode used). Furthermore, since branch prediction is used in both branch prediction modes in GB '595, both branch prediction modes result in a same address valid time. Therefore, GB '595 does not teach or suggest two modes of operation where the second mode results in a second address setup timing that allows for an earlier address valid time, as claimed in claims 10 and 16. Therefore, for at least these reasons, Applicants submit that claims 10 and 16 are patentable over GB '595.

Claims 11-13 and 17-20 all depend directly or indirectly from allowable claims 10 and 16 and are therefore allowable for at least those reasons described above with respect to claims 10 and 16.

Rejection of claims 6 and 14 under 35 U.S.C. 103(a)

Applicants respectfully submit that claims 6 and 14 are patentable over GB '595 under 35 U.S.C. 103(a). Claims 6 and 14 depend directly or indirectly from allowable claims 1 and 10, respectively, and are therefore allowable for at least those reasons stated above with respect to claims 1 and 10, respectively. Furthermore, in rejecting claims 6 and 14 over GB '595 under 35 U.S.C. 103(a), the Examiner states that "using a signal being hardwired to a predetermined state to speed up signal process is old and well known in the art." However, Applicants submit that it would not be obvious to modify the signals of GB '595 to be hardwired to a predetermined state. While a hardwired signal may increase speed of a particular signal, it also removes the flexibility of being able to change states of the signal. The signals in GB '595 cited by the Examiner to perform branch prediction need to be able to toggle states in order to properly control the logic within data processor 10 of GB '595. Therefore, for these additional reasons, claims 6 and 14 are patentable over GB '595.

Conclusion

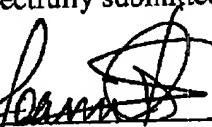
Although Applicants may disagree with statements made by the Examiner in reference to the claims and the cited references, Applicants are not discussing all these statements in the current Office Action, yet reserve the right to address them at a later time if necessary.

Applicant respectfully solicits allowance of the pending claims. Contact me if there are any issues regarding this communication or the current Application.

If Applicant has overlooked any additional fees, or if any overpayment has been made, the Commissioner is hereby authorized to credit or debit Deposit Account 502117.

Respectfully submitted,

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